Applicants have amended the Title, as well as claim 1, per the Examiner's suggestions. Accordingly, Applicants respectfully submit that the rejections and objections to the title and to claim 1 on 112 grounds have been traversed.

In the Office Action, pending claims 1-5 and 7 stand rejected under 35 U.S.C. 102 in view of the Cunningham reference, U.S. patent 6,177,697 B1 (the '697 patent). In response, Applicants respectfully submit that this reference, taken alone or in combination with any other reference of record, neither teaches nor suggests the invention as recited in the claims as presented herein.

In the invention, a trench having a depth approximating that of the isolation trenches is used to provide a trench capacitor. The capacitor trenches are formed "in a region of the semiconductor substrate in which said plurality of isolation filled trenches are absent." In the '697 reference the capacitor trench 14 is formed in the same regions as the isolation trenches 10. They are not only in the same regions; they are next to one another. The '697 reference is a divisional of the 6,087,214 Cunningham reference discussed and distinguished in paragraphs 6 and 7 of the present specification. The '697 reference utilizes isolation trenches is close proximity to the capacitor trenches to provide cell-to-cell isolation, increasing total cell area. In the invention, the capacitor trenches are formed in areas where there are no isolation trenches. This is neither shown nor suggested by the '697 reference. If anything, the '697 reference teaches away from the combination of features recited in claim 1. Accordingly, Applicants respectfully submit that the rejection of claims 1-5 and 7 as being anticipated by the '697 reference has been traversed.

In the Office Action, claims 6 and 9 stand rejected under 35 U.S.C. 103 in view of a combination of the teachings of the '697 patent and U.S. patent 5,183,774 ("Satoh"). In response, Applicants respectfully submit that the Satoh reference, taken alone or in combination with any other reference of record, neither teaches nor suggests the invention as recited in these claims. Applicants respectfully submit that the aforementioned shortcomings of the teachings of the '697 patent are not addressed by the Satoh reference. The Satoh reference is cited for establishing that

it is known to have oxide isolation at the bottom of trench capacitors. The Satoh reference makes no mention of using trench capacitors that have a depth similar to that of isolation trenches appearing elsewhere on the chip. In fact, Satoh makes no mention of trench isolation at all. That is because the trench capacitor is relied on to provide cell-to-cell isolation. Applicants claim an integrated chip in which some areas have isolation trenches and some areas have trench capacitors, the two types of trenches having the same proximate depths. This integrated structure is not suggested by the combination of '697 and Satoh, because '697 suggests the isolation trenches and the trench capacitors must be in close proximity to one another, and Satoh does not teach the use of isolation trenches at all. Nowhere in either of these references is there a suggestion of the integrated combination as recited in the subject claims. Accordingly, Applicants respectfully submit that the rejection of record to claims 6 and 9 has been traversed.

In the Office Action, claims 8 and 10 stand rejected under 35 U.S.C. 103 in view of a combination of the teachings of the '697 patent and U.S. patent 6.437,369 ("Tang"). In response, Applicants respectfully submit that the Tang reference, taken alone or in combination with any other reference of record, neither teaches nor suggests the invention as recited in these claims. Tang shows trench capacitors that extend through an SOI isolation. Applying Tang to '697 as suggested by the Examiner, Applicants respectfully submit that such a combined structure would be shallow isolation trenches and deeper trench capacitors, the isolation trenches being proximate the trench capacitors. This combination would neither teach nor suggest the invention, in that isolation trenches would be proximate the trench capacitors, and the trench capacitors would be much deeper than the isolation trenches. Both of these features of the suggested combination would tend to teach away, rather than toward, the invention as recited in the pending claims. Accordingly, Applicants respectfully submit that the rejection of record to claims 8 and 10 has been traversed.

Accordingly, Applicants respectfully request entry of the present Amendment and passage of their subject application to issuance in view thereof. Should the Examiner have any comments,

questions, or suggestions, please d not hesitate to contact the undersigned attorney at the telephone number and/or email address set forth below.

Respectfully submitted,

For: Brown et al.

By: _____

Mark F. Chadurjian
Reg. No. 30,739
Telephone: (802) 769-8843
Facsimile (802) 769-8938
Email: mchadurj@us.ibm.com

IBM Corporation, IPLaw Dept. 972E
1000 River Street
Essex Junction, VT 05452

Exhibit A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Title:

Amend the Title, as it appears on the first page and immediately above the Abstract, to read as follows:

[Method and] Structure For Scalable, Low-Cost Polysilicon DRAM in a Planar Capacitor

In the Claims:

Cancel claims 11-20.

1. A structure formed on a semiconductor substrate comprising:
a plurality of isolation filled trenches in the substrate;
a plurality of holes in the substrate, each having a plurality of sidewalls and a bottom wall, located in a region of the [a] semiconductor substrate in which said plurality of isolation filled trenches are absent, said holes having a depth proximate that of said plurality of isolation filled trenches;
insulating material present in each of said plurality of holes on said plurality of sidewalls and bottom wall; and
a conductor overfilling each of said holes and extending onto an adjacent upper surface of the substrate.